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Attorney Docket No. 20155-000100US

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

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By: Diane Damonte

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09/552983
04/21/00

ASSISTANT COMMISSIONER FOR PATENTS
BOX PATENT APPLICATION
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is the
[X] patent application of
[ ] continuation patent application of
[ ] divisional patent application of
[ ] continuation-in-part patent application of

Inventor(s)/Applicant Identifier: Patrick Christian

For: SYSTEM USING INDIRECT ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS

[X] This application claims priority from each of the following Application Nos./filing dates:
GB 0002062.8, filed January 28, 2000, the disclosure(s) of which is (are) incorporated by reference.

[ ] Please amend this application by adding the following before the first sentence: "This application is a [ ] continuation [ ] continuation-in-part of and claims the benefit of U.S. Provisional Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference."

Enclosed are:
[X] 5 page(s) of specification
[X] 3 page(s) of claims
[X] 1 page of Abstract
[X] 1 sheet(s) of [ ] formal [X] informal drawing(s).
[ ] An assignment of the invention to _____
[ ] A [ ] signed [ ] unsigned Declaration & Power of Attorney
[X] A [X] signed [ ] unsigned Declaration.
[ ] A Power of Attorney by Assignee with Certificate Under 37 CFR Section 3.73(b).
[X] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [X] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application.
[ ] Notification of change of [ ] power of attorney [ ] correspondence address filed in prior application.
[ ]

	(Col. 1)		(Col. 2)
FOR:	NO. FILED		NO. EXTRA
BASIC FEE			
TOTAL CLAIMS	11	- 20 =	*0
INDEP. CLAIMS	3	- 3 =	*0
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED			

* If the difference in Col. 1 is less than 0, enter "0" in Col. 2.

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	FEE	OR	RATE	FEE
	$345.00	OR		$690.00
x $9.00 =	$0.00	OR	x $18.00 =	
x $39.00 =	$0.00	OR	x $78.00 =	
+ $130.00 =		OR	+ $260.00 =	
TOTAL	$345.00	OR	TOTAL	

Please charge Deposit Account No. 20-1430 as follows:
[X] Filing fee $ $345.00
[X] Any additional fees associated with this paper or during the pendency of this application.
[ ] The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b)

[ ] A check for $_____ is enclosed.
2 extra copies of this sheet are enclosed.

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

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VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)) - SMALL BUSINESS CONCERN

Applicant or Patentee: Patrick Christian
Application or Patent No.: Unassigned
Filed or Issued: Herewith
Title: SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS

I hereby declare that I am:

[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below.

Name of Small Business Concern: VegaStream, Ltd.
Address of Small Business Concern: Technology Transfer Center, Silwood Park, Buckhurst Road
Ascot, Berkshire SL5 7PW ENGLAND

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS by inventor(s) Patrick Christian described in:

[X] the specification filed herewith;
[ ] Application No. _____, filed _____;
[ ] Patent No. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name: _____
Address: _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name: _____
Address: _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: PATRICK CHRISTIAN
Title of Person if Other than Owner.
Address of Person Signing: Technology Transfer Center, Silwood Park, Buckhurst Road
Ascot, Berkshire SL5 7PW ENGLAND

Signature _____ Date 11 APRIL 2005.

SF 1062860 v1

Attorney Docket No.: 20155-000100US

PATENT APPLICATION

SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS

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SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from British Patent Application No. 0002062.8 filed on January 28, 2000, the disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

This invention relates in general to digital systems and more specifically to a digital system using indirect memory addressing to perform cross-connecting of data streams.

Digital data formats are being used to represent almost every type of information imaginable. Not only are numbers, text and images represented digitally, but digital formats now include standards for voice and video. For example, standards promulgated by the International Telecommunications Union (ITU) provide standard specifications for compressing and transferring digital audio and video. The use of digital formats has distinct benefits in providing information that can be easily and accurately stored, transferred, processed and presented to human end users or electronic digital systems.

In some applications, such as telephony or video, it is desirable to provide a continuous "stream" of data in real time. This is necessary in cases where the digital data must be transferred immediately (as with telephony) or where the amount of data is so large that it is more efficient to present the data immediately as it is being received so that large buffers or other extensive storage is not necessary (as with video). Such streaming data not only needs to be transferred as quickly and as efficiently as possible, but it must be sent to particular destinations over a network. When the number of users of a network is very large, the problem of handling fast streams of data efficiently while also providing the ability to quickly and accurately deliver the streaming data to desired end users becomes complex.

The world-wide Internet has become a popular network. A great deal of effort is being focused on inventions to allow the Internet to handle streaming data while

still maintaining the Internet benefits of a flexible routing scheme and the ability to massively scale to millions of users and content providers. These abilities should allow the Internet to be successfully adapted to such applications as telephony, video, three-dimensional simulation, email, or other audio and image digital data distribution applications.

However, the nature of the Internet's "Internet Protocol" (IP) and distributed routing requires that data, and data streams, be divided into many small "packets" of information. These packets of information must be directed, or switched, at near wire-speed without undue delay. Such a switching system must be extremely flexible in handling point-to-point, point-to-multipoint, or other possible permutations of data switching. Because of the distributed nature of the Internet, many such switches are required at many points so it is necessary to make the switches operate with as little resources (e.g., memory, processing power) as possible while still achieving the desired performance.

Thus, it is desirable to provide a fast, flexible switching system that efficiently handles data transfers in a network.

SUMMARY OF THE INVENTION

The present invention uses indirect memory addressing to perform switching of digital data streams in a network. Incoming data is organized into timeslots. Each timeslot's data is stored into a predefined location in buffer memory. Indirect addressing is implemented in a crosspoint address table. The addresses stored in the crosspoint address table are used to access locations in the buffer memory so that portions of words stored in the buffer memory can be combined to form an output word destined for a predetermined timeslot.

In a preferred embodiment, 32-bit words are stored in the buffer memory. The indirect addressing allows any byte of any word in the buffer memory to be accessed and used to form an outgoing 32-bit word. The system operates on clock cycles whereby a word of incoming data is stored at the beginning of each clock cycle and four addresses are fetched from the crosspoint address table and used to access four bytes of buffer data by the end of each clock cycle. Thus, there is a word of data coming in and a word of data going out on each clock cycle. Both the buffer storage and crosspoint address table are accessed sequentially.

One embodiment of the invention provides a system for transferring data from an incoming source to an outgoing destination. The system includes buffer storage coupled to the incoming source for receiving and storing data from the incoming source; a buffer storage address generator for sequentially addressing the buffer storage so that incoming data is stored sequentially within the buffer storage; an address storage including one or more addresses for accessing the buffer storage; an address storage address generator for sequentially accessing the one or more addresses stored in the address storage; and an output stage, wherein the output stage retrieves data from the buffer storage in accordance with the one or more addresses accessed by the address generator.

Another embodiment of the invention provides a method for switching digital data streams in a network where the digital data streams include timeslots. The method includes storing incoming data in a memory in accordance with the incoming data's timeslot and indirectly accessing the memory to determine which portions of the data to output.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating the system of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 1 is a diagram illustrating the system of the present invention.

In Fig. 1, incoming data streams 110 can include data from one or more data streams. The data streams can be serial or parallel streams. The streams can be of varying data width. Serial to parallel converter 112 is used to form data word 114 for storage. Typically, the data output from the data streams is designed so that one 32-bit word is available in a "timeslot." A timeslot is an arbitrary interval of time for use in time-division-multiplexed (TDM) channels such as Mitel's ST-Bus. A popular mode would be to take 8 bits of data (one "byte" of data) from each of four streams in a single timeslot and to combine the bytes into a 32-bit word. Note that other input schemes are possible. The present invention is adaptable, in general, to any application where TDM or TDM-like communication channels are used.

Data word 114 is stored into buffer memory 118. In a preferred embodiment, buffer memory 118 is a subsection of total memory 116. However, any memory architecture may be used. For example, memory 118 may be an entire bank of memory on a separate integrated circuit chip, may be "virtual" memory on a hard disk drive or other media, may be arranged as any word, length; may be dual-port memory, etc.

Counter 128 generates addresses for the storage of data word 114 into buffer memory 118. In Fig. 1, data word 114 is shown being stored into location 138. Other examples of data words stored into memory 118 are shown at 130, 132, 134 and 136. Counter 128 increments sequentially, 4 bytes at a time, and is synchronized to the timeslots of the incoming data. Since the timeslot data arrives in sequence, each location in buffer memory corresponds to a single timeslot, in sequence. Thus, for example, buffer location 0 corresponds to timeslot 0, buffer location 1 corresponds to timeslot 1, and so on. Note that, where buffer storage 118 is part of a larger memory bank, a "base address" serves to define location 0 of the buffer storage. As is known in the art, an index into the buffer is used as the basis for accessing word locations in the buffer storage. With this design, each incoming data word is stored sequentially into the buffer storage and buffer storage locations correspond to timeslots.

Note that other incoming storage mappings are possible. For example, the incoming data words can be stored in descending order. The storage can be in reverse correspondence to the timeslot numbers. A hashing function can be implemented to map timeslots to arbitrary locations, words can be stored in multiple storage buffer locations, etc. In general, any suitable incoming storage mapping may be employed

Fig. 1 shows crosspoint address table 160 also occupying total memory 116. As described above regarding the storage buffer, other memory architectures are possible. Crosspoint address table 160 includes pre-stored addresses for accessing bytes residing in buffer storage 118. The pre-stored addresses are typically written prior to a switching session by a host processor (not shown). The pre-stored addresses define the routing of incoming timeslot data to outgoing timeslot data. Since the addresses are byte-specific they can point to any byte in any word of buffer storage 118. Thus, an outgoing word can include any byte from any of the incoming timeslots.

On each cycle, four addresses are read from crosspoint address table 160. For example, in a given cycle, addresses 162, 164, 166 and 168 are read. These addresses reference bytes 134, 132, 136 and 130, respectively. The referenced bytes are read from

storage buffer 118 and combined in byte extractor 120 to form 32-bit word 122. When it is desirable to split the outgoing data into multiple streams then parallel to serial converter 124 can be used to generate, e.g., 4 outgoing data streams 126, as shown.

Crosspoint address table 160 is accessed sequentially. In the preferred embodiment, four addresses are accessed each clock cycle, or timeslot. Naturally, any number of accesses can be employed. Also, the same options as to memory size and implementation as discussed above with respect to the buffer storage are possible.

It should be apparent that the system of the present invention can be used to arbitrarily assign any incoming data to an outgoing timeslot. Also, incoming data can be assigned to multiple outgoing timeslots. Data can be "dropped" or ignored, etc. Although the host processor in the preferred embodiment only writes to the crosspoint address table prior to the actual switching session, dynamic updating of the crosspoint address table is possible. Although the system of the present invention has been described with respect to a specific hardware configuration, many variations are possible. Components can be combined, omitted, or added. Functions can be implemented in hardware, software, or a combination of hardware and software. Incoming and outgoing data transfers need not be synchronized with each other, as where the number of outgoing timeslots differs in number from the incoming timeslots. Other variations are possible.

Although the present invention has been described with reference to specific embodiments thereof, these embodiments are merely illustrative, and not restrictive, of the invention, the scope of which is determined solely by the appended claims.

WHAT IS CLAIMED IS:

1. 1. A system for transferring data from an incoming source to an outgoing destination, the system comprising:

a buffer storage coupled to the incoming source for receiving and storing data from the incoming source;

a buffer storage address generator for sequentially addressing the buffer storage so that incoming data is stored sequentially within the buffer storage;

address storage including one or more addresses for accessing the buffer storage;

an address storage address generator for sequentially accessing the one or more addresses stored in the address storage; and

an output stage, wherein the output stage retrieves data from the buffer storage in accordance with the one or more addresses accessed by the address generator.

2. The system of claim 1, wherein the data is telephony data.

3. The system of claim 2, wherein the incoming data is organized into timeslots, wherein the buffer storage is organized so each timeslot corresponds to a unique word location in the buffer storage.

4. The system of claim 3, wherein a word location in the buffer storage is 32 bits in length.

5. The system of claim 4, wherein the addresses include bits, wherein the lower-order two bits of each address are used to identify one of four bytes in a word location in the buffer storage.

6. The system of claim 1, further comprising

a clock having a clock cycle and outputting a clock signal; and

Wherein the buffer storage and address storage address generators are coupled to a signal derived from the clock signal so that a word of data is stored into the buffer storage at the start of each clock cycle and a word of data is read out from the buffer storage by the end of each clock cycle.

7. The system of claim 1, wherein four consecutive addresses stored in the address storage are used to each identify a portion of data from one or more locations in the buffer storage.

8. A hardware switching system for routing digital data streams in a network, the hardware switching system including:

a memory for storing incoming data;

an indirect memory addressing mechanism for accessing incoming data stored in the memory; and

an output control coupled to the indirect memory addressing scheme and the indirect memory addressing mechanism for selectively outputting portions of the data in accordance with the indirect memory addressing mechanism.

9. A method for switching digital data streams in a network, wherein the digital data streams include timeslots, the method comprising:

storing the incoming data in a memory in accordance with the timeslots; and

indirectly accessing the memory to determine which portions of the data to output.

10. The method of claim 9, wherein the incoming and output data is organized into multiple timeslots, the method further comprising:

the step of storing incoming data in a memory including the substep of assigning memory locations to timeslots so that incoming data in a predetermined timeslot is stored in a predetermined memory location; and

the step of indirectly accessing the memory further comprising the substeps of:

using multiple addresses to access multiple memory locations wherein only a portion of each memory location is used; and

combining the data in the accessed multiple memory locations to form output data to be assigned to a single timeslot.

11. The method of claim 9 stored in a machine-readable medium.

SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS

ABSTRACT OF THE DISCLOSURE

A data switch uses indirect memory addressing to perform switching of digital data streams in a network. Incoming data is organized into timeslots. Each timeslot's data is stored into a predefined location in buffer memory. Indirect addressing is implemented in a crosspoint address table. The addresses stored in the crosspoint address table are used to access locations in the buffer memory so that portions of words stored in the buffer memory can be combined to form an output word destined for a predetermined timeslot.

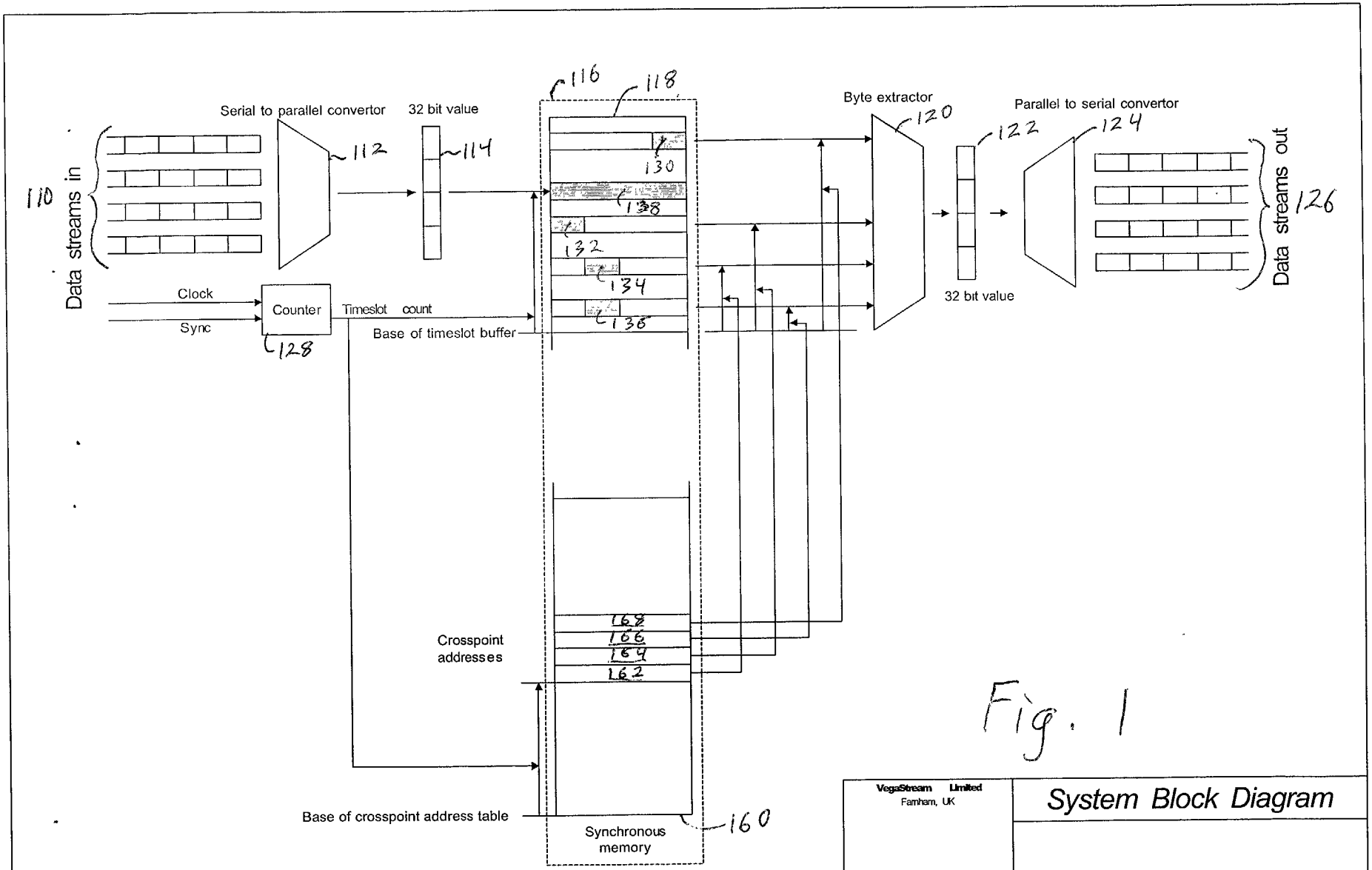

Fig. 1

VegaStream Limited Farnham, UK	System Block Diagram		
	SIZE	FSCM NO	DWG NO	REV
	SCALE		SHEET

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SYSTEM USING INDIRECT MEMORY ADDRESSING TO PERFORM CROSS-CONNECTING OF DATA TRANSFERS** the specification of which X is attached hereto or ____ was filed on _____, as Serial No. _____, and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
Great Britain	0002062.8	28 January 2000	No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

Full Name of Inventor 1:	Last Name: CHRISTIAN	First Name: PATRICK	Middle Name or Initial:	
Residence & Citizenship:	City: Farnham	State/Foreign Country: Surrey/England	Country of Citizenship: United Kingdom	
Post Office Address:	Post Office Address: 2 Clare Mead, Rowledge	City: Farnham	State/Country: Surrey/ England	Postal Code: GU10 4BJ

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1 Patrick Christian Date 11 APRIL 2020		

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